

IN THE CLAIMS

1. (original) An integrated circuit device comprising:  
an array of cells, said cells comprising a source, a drain and a gate;  
a common source line coupled with said source; and  
a source contact disposed outside of said common source line and  
coupled with said source.
2. (original) The integrated circuit device of Claim 1 comprising  
substantially straight word lines.
3. (original) The integrated circuit device of Claim 1 wherein said common  
source line has a substantially uniform width within said array of cells.
4. (original) The integrated circuit device of Claim 1 wherein said source  
contact is disposed in a row with drain contacts.
5. (original) The integrated circuit device of Claim 1 wherein said source  
contact is coupled to said common source line under a gate structure.
6. (original) The integrated circuit device of Claim 1 wherein said  
integrated circuit device comprises non-volatile memory.
7. (original) The integrated circuit device of Claim 6 wherein said non-  
volatile memory comprises a floating gate as a charge storage element.
8. (original) An integrated circuit device wherein a first region under a  
gate comprises overlapping lateral diffusions of source and drain implantation  
regions.

9. (original) The integrated circuit device of Claim 8 wherein one of said implantation regions is coupled to a first source contact.

10. (original) The integrated circuit device of Claim 8 wherein one of said implantation regions is coupled to a common source line.

11. (original) The integrated circuit device of Claim 8 further comprising a second gate, wherein a second region under said second gate comprises overlapping lateral diffusions of source and drain implantation regions.

12. (original) The integrated circuit device of Claim 11 wherein one of said implantation regions associated with said second gate structure is coupled to a second source contact.

13. (original) The integrated circuit device of Claim 11 wherein one of said implantation regions associated with said second gate structure is coupled to said common source line.

14. (original) The integrated circuit device of Claim 8 further comprising non-volatile memory.

Please cancel Claims 15-20 without prejudice.